REMARKS

Present Status of the Application

The Office Action rejected presently-pending claims 15-20. Specifically, the Office Action rejected claims 15 and 16 under 35 U.S.C. 103(a), as being unpatentable over Applicant's prior art (APA) in view of Wu (U. S. Patent 5,977,561) and Cho et al. (U. S. Patent 5,578,838). In addition, the Office Action rejected claims 18 and 19 under 35 U.S.C. 103(a), as being unpatentable over APA in view of Wu, Cho et al., and Nakajima et al. (U. S. Patent No. 6,118,140). The Office Action rejected claim 20 under 35 U.S.C. 103(a), as being unpatentable over APA in view of Wu, Cho et al., and Gardner et al. (U. S. Patent 5,872,376). Applicant has amended independent claim 15. After entry of the foregoing amendments, claims 15-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to a thin film transistor has an ultra thin polysilicon layer over a substrate, a gate structure that includes a gate layer, a gate oxide layer between the gate layer and the ultra thin polysilicon layer and a spacer on each sidewall of the gate layer, and a conductive layer over the ultra thin polysilicon layer and the gate layer adjacent to the spacers. A selective deposition, such as an in-situ silicon-germanium deposition that utilizes the difference in properties between the spacer and silicon, is conducted to form the conductive layer serving as a S/D region without additional implantation process.

Discussion of Office Action Rejections

Applicant has amended independent claim 15, which has been considered as the product by process claim. No new matter is added. No new issue has been raised.

Considering the present invention as a whole particularly in fabricating the TFT, the present invention uses the spacer 208 to create the contrast surface with respect to the gate layer 206 and the polysilicon layer 202. The spacer 208 then is allowed a selective conductive layer 210 to almost or completely only formed on the gate layer 206 and the polysilicon layer 206. ***In other words, the spacer 208 has its particularly role to adapt the selective conductive layer 210. The spacer 208 and the selective conductive layer 210 are working together and can not be separately considered.***

Further still, the selectively 210 is directly servers as the source/drain region. This inherently implies that no additional implantation process is necessary. It is believed that the amended claim 15 has overcome the issue of product-by-process.

With respect to claims 15-16, independent claim 15 recites the feature as follows:

> Claim 15. A thin film transistor structure, comprising:
> an insulating substrate;
> a polysilicon layer over the substrate;
> a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each side of the gate layer, ***wherein the spacer with respect to a surface of the gate dielectric layer and a surface of the polysilicon layer forms a contrast surface***; and
> ***a selective conductive layer over the gate layer and the polysilicon layer adjacent to the spacers based on the contrast surface, wherein the selective conductive layer adjacent to the spacers directly serves as a source/drain region*** *(emphasis added).*

When considering the spacer and the selective conductive layer together as a whole, the spacer is used to produce the contrast surface for adapting the selective conductive layer. *Here, it should be also noted that the source/drain regions (the selective conductive layer over the gate layer and the polysilicon layer) form the selective conductive layer is separated by the spacer as recited in claim 15.* The contrast surface from the spacer is the effective limitation (in response to the Office Action).

In re APA (FIG. 1B), no spacer is disclosed. The source/drain regions are in the same polysilicon layer 104. Therefore, even if a usual spacer is used, APA still cannot be modified into the claimed invention.

In re Wu, the spacer 24 is necessary to be doped, so as to form the ultra-shallow source/drain junction 28, 30 (col. 4, lines 33-39; lines 55-65) due to the diffusion effect in the thermal process. It is clear that the spacer 208 of the present invention has functioned differently from the spacer 24 of Wu, when considering the claimed invention as a whole. The contrast surface is not disclosed by Wu, and the spacer 208 of the claimed invention is not absolutely required being doped for later use to form the source/drain junctions.

Therefore, Wu failed to supply the missing features in APA. Also and, the spacer 24 of Wu cannot separate the polysilicon layer 104 of APA into two source/drain regions. The spacer 24 functions differently.

In re Cho, et al. (Figs. 4-6; col. 4, lines 53-55), the semiconductor layer 14 ***is implanted with impurity (fig. 5 and fig. 6) to form the source/drain regions***. Again, the source/drain regions are existing in the same layer without separation. Therefore, Cho et al. failed to supply the missing features in APA and Wu.

With respect to claim 17-20, the Office Action further refers to Nakajima et al. and Gardner et al. However, both Nakajima et al. and Gardner et al. failed to further supply the missing features in APA, Wu, and Cho et al..

For at least the foregoing reasons, Applicant respectfully submits that independent claim 15 patently defines over the prior art references, and should be allowed. For at least the same reasons, dependent claims 16-20 define over the prior art references as well.

Also and, no new issue is raised and the Office Action should not be FINAL.

CONCLUSION

For at least the foregoing reasons, it is believed that pending claims 15-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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